

**IEEE 802.11  
Wireless Access Method and Physical Specification**

Title: **Summary of DS/GFSK High Speed 2.4 GHz PHY**

Date: November 10, 1997

Author: Dean Kawaguchi

Symbol Technologies, Inc.  
2145 Hamilton Ave  
San Jose, CA. 95125  
Telephone: (408)369-2629  
FAX: (408)369-2737  
email: DeanK@psd.symbol.com

## Review of DS/GFSK Proposal

### **DS/GFSK addresses key requirements**

- Interoperability with both FH and DS
  - Hopping and non hopping modes, hopping based on FH PHY sequences
- Interference immunity in ISM band
  - GFSK is most bandwidth efficient of binary modulations (1.1 \* chip rate)
  - Hopping over 8 channels in 5 Mbps mode, 4 in 10 Mbps mode
- Multipath robustness
  - Good capture effect of FSK + DS spreading
- Good sensitivity performance
  - 5 Mbps mode same as 1 Mbps FH, 10 Mbps 3 dB worse
- Low speed preamble for interoperability, high speed for throughput
  - Both possible with fast acquisition of GFSK
- Low cost and need for architectural options
  - Constant amplitude, more efficient power amplifier

# High Speed PHY Proposal

**A succinct summary of the proposed high speed DS PHY is as follows:**

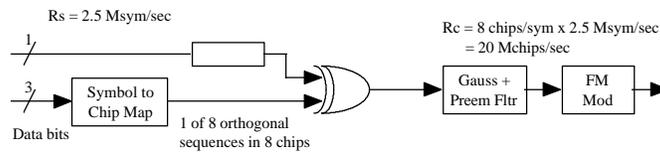
- DS spreading: 4 bits/symbol and 8 chips/symbol bi-orthogonal Walsh codes
- Modulation: Binary GFSK with deviation  $h=0.7$ ; 1.5 dB preemphasis
- Data rates: 1.25 Msym/sec (5 Mbps) and 2.5 Msym/sec (10 Mbps)
- Chipping rates: 10 Mcps and 20 Mcps
- Bandwidths: 11 MHz and 22 MHz
- Channelization: 8 channels w/10 MHz spacing, 4 channels with 20 MHz spacing

# DS Spreading Format

**The DS spreading formats used by Harris and Micrilor uses simple yet effective bi-orthogonal Walsh codes**

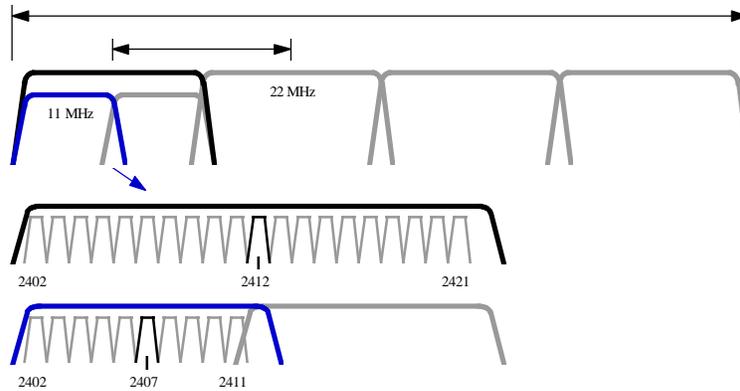
**The 8 chips per symbol used by Harris is more bandwidth efficient which is crucial to satisfy the interference fighting channelization mentioned earlier**

**The 4 bits/8 chips per symbol used at 1.25 (or 1.375) Msps and at 2.5 Msps would produce 5 and 10 Mbps at a chipping rate 10 and 20 Mcps**



# Hopping and interoperability with 1&2 Mbps FH PHY

The hopping can be synchronized to interoperate with the 1 and 2 Mbps FH PHY



# Interoperability with FH PHY

**Interoperability preamble using FH 1 Mbps with rate switch sync period**

**HS preamble mode for max throughput and operation in HS capable units only environments**

- HS preamble is -16  $\mu$ s including time for diversity selection

**In either mode, CCA on all 1 MHz channels in wideband channel possible at reduced sensitivity**

**Full sensitivity on 1 MHz channel associated on with digital implementations**

## Low cost, many architectural options

---

---

**An FSK system has been the lowest cost due to the simplicity, inherent robustness, and use of nonlinear components.**

**There are many options and design optimizations which will allow manufacturers to optimize for various applications and price/performance tradeoffs.**

**Digital implementation with parallel demod, subband tuning for 1 MHz channel requires only additional gates in ASIC**

**1 MHz SAW for full selectivity performance 1/2 Mbps only mode, tune synthesizer to channel**

**Existing DS RF and IF chip sets may also be used**

**Intellectual property - Walsh codes and binary GFSK on wireless is probably not patentable any more.**