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Table 4-38: Inter.5-*-0.0004 Tc0.002: Pi5-6.....3(in...-180.p5.881904.....)-220.1(64)]TT*[(Tabl

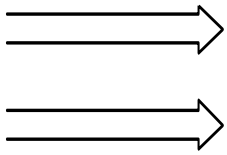
- Parity Generation (PAR), Parity Error Detection (PERR# and SER#)

2.3 PCI Target Unit

WISHBONE bus is accessible to PCI agents through PCI target unit of the bridge. PCI target unit provides two to five images of WISHBONE side memory space. Each of these images is selected with address provided during address cycle on the PCI bus compared with base address masked with mask value stored in PCI configuration registers. Each image can be mapped into I/O or memory space.
Writes through PCI target unit are handled as posted writes while reads are pre-fetched. Posted writes are stored in PCIW_FFR_FF

2.3.1 PCI Target Unit Architecture

This section describes architecture of PCI target unit. Detailed description is provided in following sections.



FIFO is structured from more than one FIFO lines. The number of FIFO lines is the number of FIFO's depth, and it can be configurable (how the number of FIFO depth is defined will be discussed in detail in design document and implementation notes). The structure of one FIFO line is well described in Figure 2-4. It consists of 4 control bits (how they are used, will be described in detail in design document, e.g. one bit is used to sign last data of the burst transfer etc.), 4 command or byte enable bits (coding will be described in detail in design document), 32 address or data bits.

3

3.3 1.r9

- The burst crosses a resource boundary (or a resource boundary occurs).

PCI Target unit abnormally terminates transfer, when it detects a fatal error or it will never be able to complete the requested transfer, with Target-Abort:

- Master initiates a non-valid combination of AD(1:0) and BE#(3:0) when

4

Registers

Code	Offset	Width	Access	Description
P_BA4	0x020 and 0x138	32	R/W	PCI Image4 Base Address Register
P_AM4	0x13C	32	R/W	PCI Image4 Address Mask Register
P_TA4	0x140	32	R/W	PCI Image4 Translation

Register layout:

Bits descriptions:

Bit number	Name	Description
31	Image Enable & Address Mask(31)	Bit must be set for image to be enabled. If bit is 0, corresponding image is not enabled. This bit is also used in Address Masking – that's how a limit of 2GB per image is implemented (at least ADDR_I(31)) must be compared with BA for each image.

30 – 12 22.8.3aie0008 Tw[(30e5* ne(h12 22.8)412 maindqET[(30e5* ne(4(bi2)4.f)2)4. B)6ET(x00084(f))2

Vendor ID, Device ID, Command, Status, Revision ID, Class Code and Header Type

Bit number	Implemented	Description
6	ã	

Bit number

Bits descriptions:

Bit number

Address mask registers – P_AM1 – P_AM5

PCI Erroneous Address Register – P _ERR_ADDR

Width	Access	Reset	Description

Name

5.2 WISHBONE Interface

The SoC interface is a WISHBONE Rev B compliant interface. PCI IP core's

CLK_I
ADDR_I[31:0]
SDATA_O[31:0]
SDATA_I[31:0]
WE_I
SEL_I[3:0]
STB_I
ACK_O
CYC_I
ERR_O
RTY_O

www.a201SEL64l6e63.0(a20/T47)49938 Twww48/7597e63.58l28.a201SEL643.1l9026.9938 Twww48/7

If Error Reporting is enabled and transaction is a posted write, address, bus command, data and byte enables are stored in corresponding registers (See chapter 3.2.3) and WISHBONE slave unit locks out all but configuration space accesses until proper Error

CLK_I
ADDR_O[31:0]
MDATA_I[31:0]
MDATA_O[31:0]
WE_O
SEL_O[3:0]
STB_O
ACK_I

other PCI agents. If GUEST is defined, this Base Address is set by other PCI