marca - McAdam's RISC Computer Architecture Instruction Set Architecture

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1 General

- 16 16-bit registers, r0 . . . r15
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stvec r1, n4	11111101	$r1 \rightarrow$ interrupt vector $n4, 0 \leq n4 \leq 15$
jmp r1	111111100000	$r1 \rightarrow pc$
jmpz r1	111111100001	$Z = 1 \quad r1 \rightarrow pc$
jmpnz r1	111111100010	$Z = 0 \quad r1 \rightarrow pc$
jmple r1	111111100011	$(Z = 1) \quad (N = V) \quad r1 \rightarrow pc$
jmplt r1	111111100100	$(Z = 0) \quad (N = V) \quad r1 \rightarrow pc$
jmpge r1	111111100101	$(Z = 1) \quad (N = V) \quad r1 \rightarrow pc$
jmpgt r1	111111100110	$(Z = 0) \quad (N = V) \quad r1 \rightarrow pc$
jmpule r1	111111100111	$(Z = 1) \quad (C = 1) \quad r1 \rightarrow pc$
jmpult r1	111111101000	$(Z = 0) \quad (C = 1) \quad r1 \rightarrow pc$
jmpuge r1	111111101001	$(Z = 1) \quad (C = 0) \quad r1 \rightarrow pc$
jmpugt r1	111111101010	$(Z = 0) \quad (C = 0) \quad r1 \rightarrow pc$
intr n4	111111101011	interrupt vector $n4 \rightarrow pc, pc \rightarrow ira, flags \rightarrow shflags, 0 \leq n4 \leq 15$
getira r1	111111101100	$ira \rightarrow r1$
setira r1	111111101101	$r1 \rightarrow ira$
getfl r1	111111101110	$flags \rightarrow r1$
setfl r1	111111101111	$r1 \rightarrow flags$
getshfl r1	111111110000	$shflags \rightarrow r1$
setshfl r1	111111110001	$r1 \rightarrow shflags$
reti	1111111111110000	$ira \rightarrow pc, shflags$ 1 111111110011 11111101010 1111111110011

2.2 Instruction formats

The following formats for instructions are to be used:

Bits 15 . . . 12	Bits 11 . . . 8	Bits 7 . . . 4	Bits 3 . . . 0
Opcode	r3		