# $I^2C$-Master Core Specification

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# *Revision History*

| Rev. | |
|---|---|

### 3.2.6 Status register

| Bit # | Access | Description |
|---|---|---|
| 7 | R | RxACK, Received acknowledge from slave.<br>This flag represents acknowledge from the addressed slave.<br>‘1’ = No acknowledge received<br>‘0’ = Acknowledge received |
| 6 | R | BuserI13.492e |

# 5

# Architecture

The I2C core is built around four primary blocks; the Clock Generator, the Byte

# 5.3 Bit Command Controller