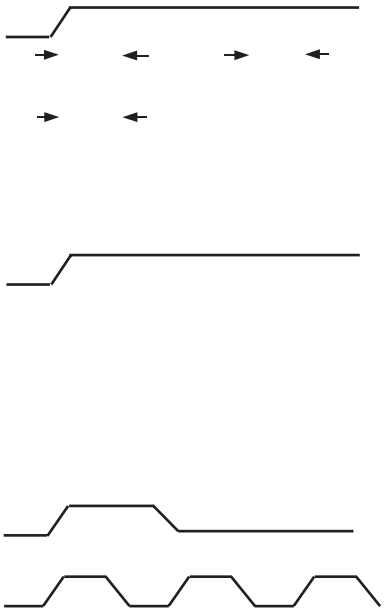
AD1896*

TIMING DIAGRAMS



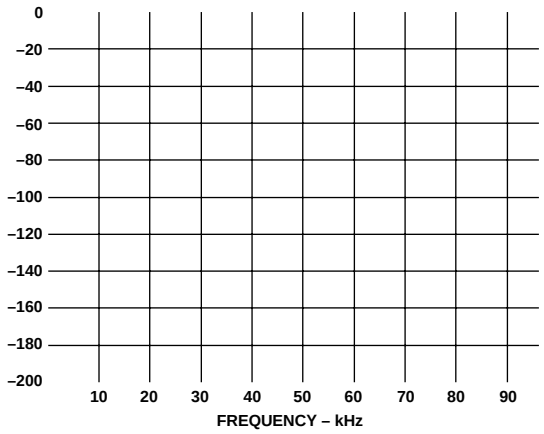
DIGITAL FILTERS (VDD_CORE = 3.3 V □ 5%, VDD_IO = 5.0 V □ 10%)

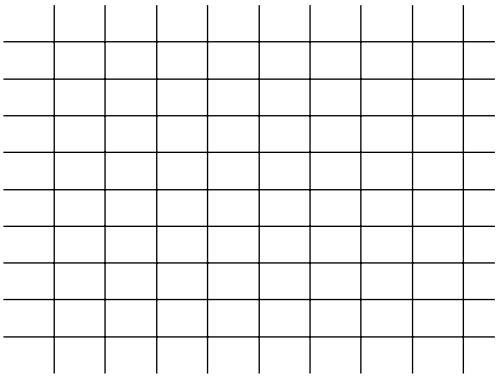
Parameter	Min	Typ	Max	Unit
Pass-Band			0.4535 f_{S_OUT}	Hz
Pass-Band Ripple			±0.016	dB
Transition Band	0.4535 f_{S_OUT}		0.5465 f_{S_OUT}	Hz
Stop-Band	0.5465 f_{S_OUT}			Hz
Stop-Band Attenuation		–125		dB
Group Delay	Refer to the Group Delay Equations section.			

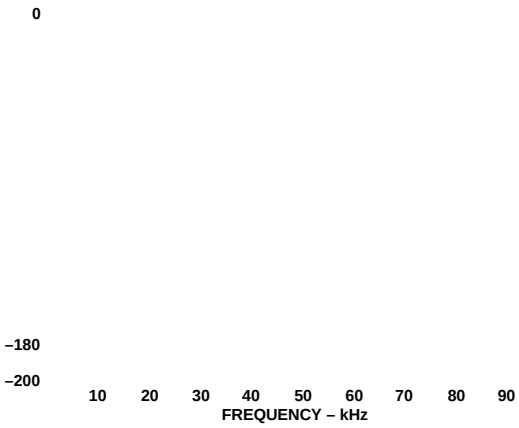
Specifications subject to change without notice.

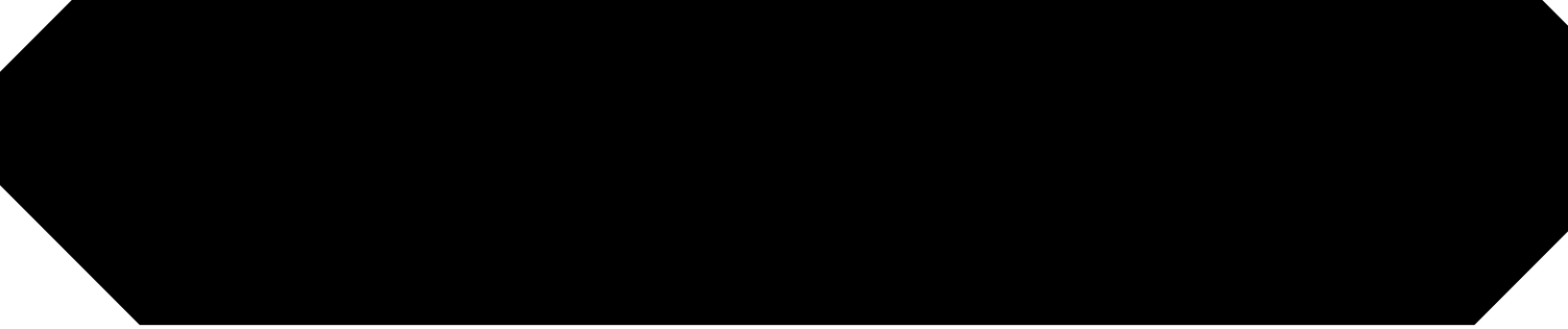
DIGITAL I/O CHARACTERISTICS (VDD_CORE = 3.3 V

PIN CONFIGURATION

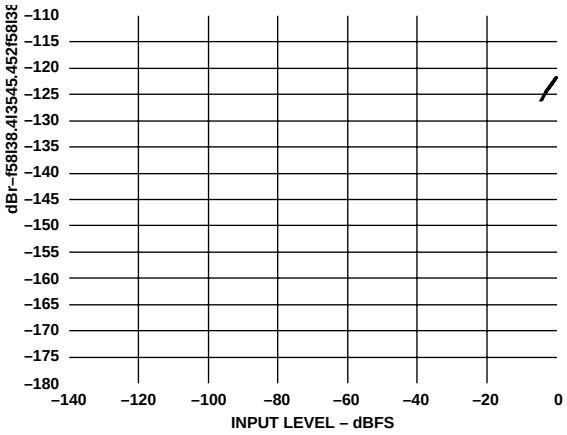

0
–20
–40
–60
–80
–100
–120
–140
–160
–180
–200
10
20
30
40
50
60
70
80
90
FREQUENCY – kHz

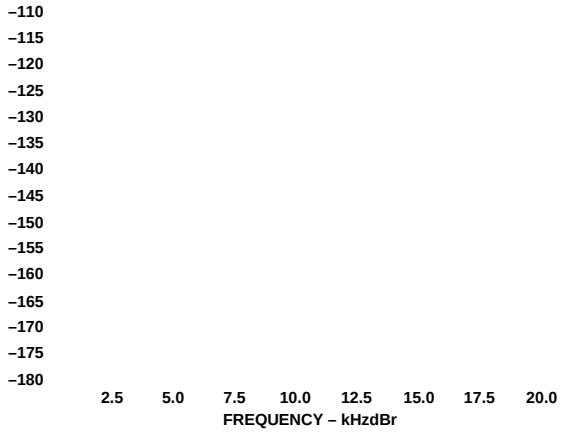



0
–180
–200
10
20
30
40
50
60
70
80
90
FREQUENCY – kHz



–5


–110
–115
–120
–125
–130
–135
–140
–145
–150
–155
–160
–165
–170
–175
–180
–140
–120
–100
–80
–60
–40
–20
0
INPUT LEVEL – dBFS


–110
–115
–120
–125
–130
–135
–140
–145
–150
–155
–160
–165
–170
–175
–180
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
FREQUENCY – kHz
dBr

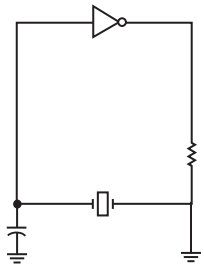
(*Continued from Page 1*)

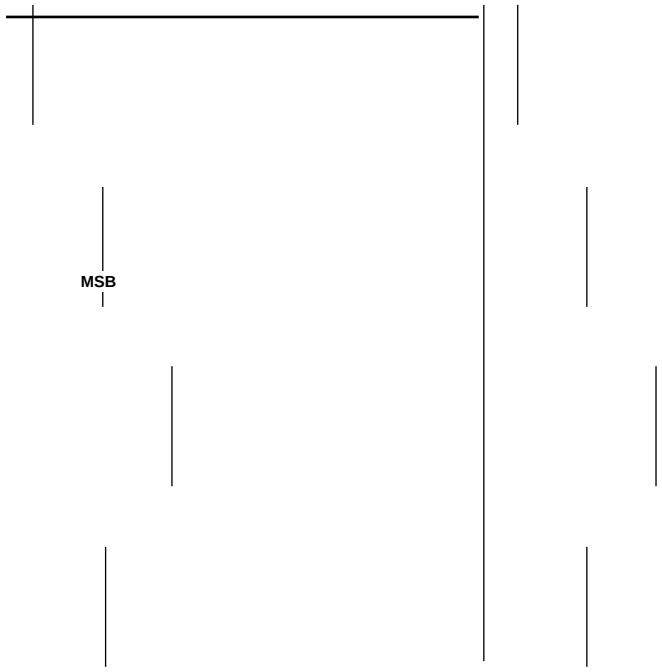
The digital servo loop measures the time difference between the input and output sample rates within 5 ps. This is necessary in order to select the correct polyphase filter coefficient. The digital servo loop has excellent jitter rejection for both input and output sample rates as well as the master clock. The jitter rejection begins at less than 1 Hz. This requires a long settling time whenever

ASRC FUNCTIONAL OVERVIEW
THEORY OF OPERATION

Asynchronous sample rate conversion is converting data from one clock source at some sample rate to another clock source at the same or a different sample rate. The simplest approach to an asynchronous sample rate conversion is the use of a zero-order hold between the two samplers shown in Figure 4. In an asynchronous system, T2 is never equal to T1 nor is the ratio between T2 and T1 rational. As a result, samples at f_{S_OUT} will be repeated or dropped producing an error in the resampling process. The frequency domain shows the wide side lobes that result from this error when the sampling of ft43_OUT

The digital servo loop is essentially a ramp filter that provides the initial pointer to the address in RAM and ROM for the start of the FIR convolution. The RAM pointer is the integer output of the ramp filter while the ROM is the fractional part. The digital servo loop must be able to provide excellent rejection of jitter on the f





TDM MODE APPLICATION

In TDM mode, several AD1896s can be daisy-chained together and connected to the serial input port of a SHARC DSP. The AD1896 contains a 64-bit parallel load shift register. When the LRCLK_O pulse arrives, each AD1896 parallel loads its left and right data into the 64-bit shift register. The input to the shift register is connected to TDM_IN, while the output is connected to SDATA_O. By connecting the SDATA_O to the TDM_IN of the next AD1896, a large shift register is created, which is clocked by SCLK_O.

The number of AD1896s that can be daisy-chained together is limited by the maximum frequency of SCLK_O, which is about 25 MHz. For example, if the output sample rate, f_S, is 48 kHz, up to eight AD1896s could be connected since 512 ¥ f_S is less than 25 MHz. In master/TDM mode, the number of AD1896s that can be daisy-chained is fixed to four.

Serial Data Port Master Clock Modes
Either of the AD1896 serial ports can be configured as a master serial data port. However, only one serial port can be a master while the other has to be a slave. In master mode, the AD1896 requires a 256 ¥ f_S

OUTLINE DIMENSIONS

28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

0.2