

10_100_1000 Mbps

OpenCores

Revision History

Rev.	Date	Author	Description
0.1	12/13/05	Jon Gao	First Draft

At the same time, the transmit state machine will enter pause mode and delay packet send for 10 slot time.

1.5 Source MAC replace

edit CPU.dec as following:

12070001

12080030

120a0001

180a0000

18080031

18090001

180a0001

180a0000

18080032

18090002

180a0001

180a0000

18080033

18090003

180a0001

180a0000

18080034

18090004

180a0001

180a0000

18080035

18090005

180a0001

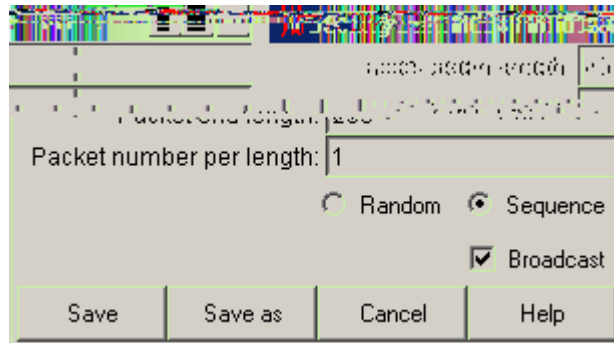
180a0000

received packet is:

0x000: 10 11 12 13 14 15 30 31

1.7 Broadcast filter test

Setting Stimulus as following windows:



Setting Reg config as following windows:

